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09/542,174	04/04/2000	Hung-Mao Lin	1532P	5884

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EXAMINER	
DOOLEY, MATTHEW C	

ART UNIT	PAPER NUMBER
2133	7

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/542,174	LIN ET AL.	
	Examiner	Art Unit	
	Matthew C. Dooley	2133	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 April 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1-3 are objected to under section 608.02(l) in the M.P.E.P. Portions of the figures are not consistent with the requirements as set forth in the aforementioned section, specifically with regards to "Every line, number, and letter must be...sufficiently dense and dark, and uniformly thick and well defined." Correction is required.

Response to Arguments/Amendments

2. Applicant's arguments filed 12/11/03 have been fully considered but they are not persuasive. Arguments and amendments were made with respect to claims 1, 8, and 15 and are dealt with below.

3. Claims 2 and 3 have been cancelled and will not be dealt with further.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 15, 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Ohhata et al., U.S. 5,402,377.

As per claim 1:

Ohhata teaches of a secondary memory array that provides a cache for a memory unit (Fig.2). Inclusive in the taught method of increasing the yield of the memory cell is a method of determining when an access is made to a failed memory bit location in the

memory cell, and then substituting a memory location in the cached memory location when the defective location is accessed (Col.2: 55-68). Claim limitations of previously rejected claims 2 and 3 have been rewritten into claim 1. However, Ohhata teaches to the rewritten limitation of identifying each failed bit location and storing an indication of the failed memory bit location in the cache memory cell (Col.2: 60-69). Moreover, it is argued that there is no lookup table in the references. However, the cached memory array of Ohhata acts as a lookup table (Fig.2; Col.2: 60-67). The language of claim 1 requires two actions for increasing the yield of usable memory locations in a memory device, namely, identifying a failed bit location in the memory device, and storing a failed bit location in the cache, in a lookup table format. Ohhata teaches to identifying a failed bit location in the memory device, and storing a failed bit location in the cache (Fig.2; Col.2: 60-67). The cache allows for cell defect signals to be produced based on the aforementioned stored defect information, therefore, providing all the functionality of a look-up table, that is, storing and retrieving data related to the identification of a failed bit location and identification of the address of said failure location (Col.15: 42-52).

As per claim 15:

Claim 15 has been amended, however still remains the corresponding apparatus claim to method claim 1. As such, analogous reasoning can be used in the rejection of claim 15 as was used in the rejection of claim 1 above.

As per claim 18:

Ohhata teaches to identifying each failed bit location in the memory unit and storing the failed bit locations in a cache (Col.2: 60-69).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 4, 6-7,16-17, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohhata et al., U.S. 5,402,377, in view of Bhavsar et al., U.S. 6,408,401.

As per claim 4:

Not explicitly taught by Ohhata is a method utilizing a comparison of the failed bit locations. Bhavsar teaches to a bit failure location comparison used for the purpose of identification of a faulty memory cell (Col.2: 10-16). It would have been obvious for one of ordinary skill in the art at the time of the invention to make use of the comparison techniques taught by Bhavsar in conjunction with the method of Ohhata because the explicit comparison methodology allows for precise notification of faulty memory cells (Bhavsar, Col.2: 10-12).

As per claim 6:

The circuitry of Bhavsar allows for the cache to be of a SRAM type (Col.2: 6-8).

As per claim 7:

The circuitry of Bhavsar allows for the cache to be of a DRAM type (Col.2: 6-8).

As per claim 16:

Claim 16 is the corresponding apparatus claim to method claim 7. As such, analogous reasoning can be used in the rejection of claim 16 as was used in the rejection of claim 7 above.

As per claim 17:

Claim 17 is the corresponding apparatus claim to method claim 6. As such, analogous reasoning can be used in the rejection of claim 17 as was used in the rejection of claim 6 above.

As per claim 19:

Claim 19 is the corresponding apparatus claim to method claim 4. As such, analogous reasoning can be used in the rejection of claim 19 as was used in the rejection of claim 4 above.

8. Claims 5, 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohhata et al., U.S. 5,402,377, in view of Douceur, U.S. 5,838,893.

As per claim 5:

Ohhata does not teach of a method including a pre-scan operation on the memory array for the purpose of identifying a failed memory cell location. Douceur teaches that it is known to make a determination of faulty memory cell locations upon device startup (Col.1: 47-56). It would have been obvious for one of ordinary skill in the art at the time of the invention to utilize the testing methodology set forth by Douceur in the method provided by Ohhata because testing at startup allows for an early determination to be made on the error status of the memory cell location (Douceur, Col.1: 55-56).

As per claim 8:

Shown above is a combination of Douceur and Ohhata that allows for a pre-scan operation to be performed whereby a memory location is swapped into a cache location. Moreover, it has been shown above that Ohhata teaches to the storage of each failed bit location in a look-up table (Col.2: 60-67).

As per claim 9:

The cache memory array of Ohhata is between a primary memory array, and a memory control unit (Fig.2).

As per claim 10:

The cached memory array of Ohhata acts as a lookup table (Fig.2).

As per claim 11:

The memory control unit of Ohhata is responsible for the swapping of memory locations between the primary array and the cache memory array upon detection of a failed memory location (Col. 2: 55-69).

As per claim 12:

The memory control unit of Ohhata is responsible for the swapping of memory locations between the primary array and the cache memory array (Col. 2: 55-69).

9. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohhata et al., U.S. 5,402,377, in view of Douceur, U.S. 5,838,893, and in further view of Bhavsar et al., U.S. 6,408,401.

As per claim 13:

It has been shown above that it would have been obvious for one of ordinary skill in the art at the time of the invention to utilize the testing methodology set forth by Douceur in the method provided by Ohhata because testing at startup allows for an early determination to be made on the error status of the memory cell location (Douceur, Col.1: 55-56). Likewise, it has been shown above that it too would have been obvious for one of ordinary skill in the art at the time of the invention to make use of the comparison techniques taught by Bhavsar in conjunction with the method of Ohhata because the explicit comparison methodology allows for precise notification of faulty memory cells (Bhavsar, Col.2: 10-12). Moreover, it was shown that the circuitry of Bhavsar allows for the cache to be of a DRAM type (Col.2: 6-8). The combinations of the methods demonstrated above would have been obvious for one of ordinary skill in the art to make at the time of the invention because these combinations allow for early error location determinations to be made on the error status of the memory cell location, wherein the precision of the memory cell error notification becomes more precise, thus leading to better overall system functionality.

As per claim 14:

It has been shown above that it would have been obvious for one of ordinary skill in the art at the time of the invention to utilize the testing methodology set forth by Douceur in the method provided by Ohhata because testing at startup allows for an early determination to be made on the error status of the memory cell location (Douceur, Col.1: 55-56). Likewise, it has been shown above that it too would have been obvious for one of ordinary skill in the art at the time of the invention to make use of the comparison

techniques taught by Bhavsar in conjunction with the method of Ohhata because the explicit comparison methodology allows for precise notification of faulty memory cells (Bhavsar, Col.2: 10-12). Moreover, it was shown that the circuitry of Bhavsar allows for the cache to be of a SRAM type (Col.2: 6-8). The combinations of the methods demonstrated above would have been obvious for one of ordinary skill in the art to make at the time of the invention because these combinations allow for early error location determinations to be made on the error status of the memory cell location, wherein the precision of the memory cell error notification becomes more precise, thus leading to better overall system functionality.

10. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohhata et al., U.S. 5,402,377, in view of in view of Bhavsar et al., U.S. 6,408,401, and Torrance et al. "A 33 GB/s 13.4Mb Integrated Graphics Accelerator and Frame Buffer," IEEE International Solid-State Circuits Conference 1998.

As per claim 20:

Ohhata teaches of a secondary memory array that provides a cache for a memory unit (Fig.2). Inclusive in the taught system for increasing the yield of the memory cell is a means for determining when an access is made to a failed memory bit location in the memory cell, and then substituting a memory location in the cached memory location when the defective location is accessed (Col.2: 55-68). The circuitry of Bhavsar allows for the cache to be of a DRAM type (Col.2: 6-8). Moreover, Torrance teaches that a system with a memory module can be utilized in conjunction with a graphics accelerator

(Fig.2). Therefore, it would have been obvious for one of ordinary skill in the art to combine graphic accelerator circuitry into the device of Ohhata, as adjusted above in the combination with Bhavsar, because Ohhata allows for the test mapping of the memory array circuit, a testing methodology which is cited as by Torrance as a means for testing the embedded memory cell of a graphics accelerator.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Dooley whose telephone number is (703) 306-5538. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew Dooley
Examiner AU 2133
03/12/04

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